Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (Cancelled).

2 (Currently Amended): A substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel including a plurality of device areas, each device area having a die attach pad and a plurality of contacts, wherein each die attach pad includes a die support surface and a **uniform** peripheral ledge that is recessed relative to the die support surface wherein the **uniformly recessed** peripheral ledges extend around the outer edges of the die attach pads; and

a plurality of semiconductor dice, each die being attached to the die support surface of an associated die attach pad using an adhesive, wherein a portion of each semiconductor die extends beyond an outer edge of its associated die attach pad, and wherein the ledge is configured to retain an amount of the adhesive.

3 (Original): The substrate panel of claim 2 wherein each die attach pad has a second surface opposite to the die attach surface, wherein the area of the die attach surface is less than the area of the second surface.

4 (Previously Presented): A substrate panel as recited in claim 2 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pads.

5 (Original): A substrate panel as recited in claim 4 further comprising an encapsulant applied to the lead frame panel, wherein the second surfaces of the die attach pads and the bottom surfaces of the contacts are exposed on an outer surface of the encapsulant, and wherein the peripheral ledges retain amounts of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

6 (Previously Presented): The substrate panel of claim 2 wherein at least some of the semiconductor dice are down bonded to the respective ledges of their associated die attach pads.

7 (Previously Presented): The substrate panel of claim 2 wherein the lead frame panel comprises a matrix of tie bars arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas are separated only by the tie bars.

8 (Cancelled).

9 (Currently Amended): A packaged integrated circuit, comprising:

a substrate having a die attach pad and a plurality of contacts, the die attach pad having an upper surface and a **uniformly recessed** peripheral ledge ~~**proximate to the upper surface, wherein the peripheral ledge is**~~ located proximate to, and surrounding, an outer edge of the upper surface **and configured such that the uniformly recessed peripheral ledge extends to an outer edge of the die attach pad;**

a semiconductor die mounted on the upper surface with an adhesive;

wherein a portion of the die extends beyond an outer edge of the upper surface; and

wherein the peripheral **ledge** ~~**area**~~ is configured to retain a portion of the adhesive so as to inhibit a flow of the adhesive from the die attach pad.

10 (Currently Amended): The integrated circuit of claim 9 wherein the die attach pad has a lower surface opposite to the upper surface, the peripheral **ledge configured** ~~**area located**~~ so that the area of the upper surface is less than the area of the lower surface.

11 (Previously Presented): The integrated circuit of claim 9 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pad.

12 (Original): The integrated circuit of claim 11 further comprising an encapsulant applied to the substrate and the semiconductor die, wherein a lower surface of the die attach pad is exposed on an outer surface of the encapsulant, and wherein the peripheral ledge retains an amount of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

13 (Previously Presented): The integrated circuit of claim 9 wherein the die is down bonded to the peripheral area.

14-15 (Withdrawn).

16 (Currently Amended): A substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel including a plurality of device areas, each device area having a plurality of contacts arranged around a die attach pad, wherein each die attach pad includes a die support surface and a recessed ledge **portion** that is lower than die support surface and extends **uniformly to ~~along~~** an edge of the die attach pad.

17 (Currently Amended): The substrate panel of claim 16 wherein the peripheral **recessed** ledge**[[s]]** **portions** extend **uniformly** ~~**entirely**~~ around **all of** the outer edges of the die attach pads.

18 (Currently Amended): The substrate panel of claim 17 wherein a plurality of semiconductor dice are attached to the die support surface of each die attach pad using an adhesive layer, wherein a portion of each semiconductor die extends beyond an outer edge of its associated die attach pad, and wherein the ledge **portion** is configured to retain an amount of the adhesive.

19 (Currently Amended): The substrate panel of claim 18 wherein each of the semiconductor **[[die]]** **dies** are electrically connected with the plurality of contacts arranged around the die and wherein each die and associated electrical connections to the contacts are encapsulated.